Embedding of Chips for System in Package realization – Technology and Applications

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ABSTRACT

In this paper the realization of packages and System-in-Packages (SIP) with embedded components will be described. Embedding of semiconductor chips into substrates has several advantages. It allows a very high degree of miniaturization, due to the possibility of sequentially stacking of multiple layers containing embedded components. A further advantage is the beneficial electrical performance by short and geometrically well controlled interconnects. In addition the embedding gives a homogeneous mechanical environment of the chips, resulting in good reliability.
Furthermore this technology is also extended for high frequency, automotive radar application. Here the use of RF compatible materials is essential. Adaption of this technology towards the RF compatibility will be described, as well as first realized demonstrators.

As a result of the increasing interest in implementing embedding technologies in an industrial environment, a newly established European project "HERMES" will focus mainly on industrial adaptation of embedding technologies with an additional scope of furthering also the existing technological capabilities at prototype level. The goal is to realize a new integrated manufacturing concept to offer low cost solutions for high density electronic systems. New manufacturing and technological challenges arise from the industrialization of component embedding technologies. The new process should combine PCB (Printed Circuit Board) technology and die assembly in one production process in order to benefit the most from large-area processing and high-density packaging.

Keywords: 3D packaging, embedded chips, Chip in Polymer, System in Package

INTRODUCTION

Technologies for the embedding of active and passive components into build up layers of substrates have attracted increasing attention during recent years. Different embedding technologies have been developed due to different requirements with respect to electrical performance, chip dimensions, and interconnection [1], [2], [3], [4]. Some of those technologies are now mature enough for ramp up in large scale production in the mobile communication sector.
Fraunhofer IZM and TU Berlin together are developing technologies for embedding of active chips and passive components for SiP applications. The first development was the so-called Chip in Polymer technology, which allows realization of SIPs as well as boards with integrated components [5]
In the EU funded project HIDING DIES [6], [7] industrial and academic partners did combine their expertise and achieved a stable technology platform for highest integration. The embedding technology has used successfully lamination of RCC and laser via interconnects to chip pads. At PCB manufacturing level, 50 µm thin chips have been embedded with pitches down to 200 µm in up to 18"x24" panels. At prototype level, embedding of chips down to 100 µm pitch was realized. Innovative methods for embedding of thick chips have been demonstrated by using prepregs in combination with RCC. The HIDING DIES project has successfully shown the immense technological capabilities of chip embedding for miniaturized electronic systems and therefore has sparked tremendous interest for industrial adoption.
Within the HIDING DIES project, the generic technology was further developed to offer versatile solutions for the realization of 3D-SiP modules. As a successor of HIDING DIES, the new EU-funded project "HERMES" has inaugurated with wide participation of European industries and research institutes with a broader scope of furthering the embedding technology borders at R&D level and more importantly of bringing embedding technology in real manufacturing PCB production.
This paper will give an overview about the Chip in Polymer embedding technology and introduces the new challenges and ideas on R&D level to overcome the rising fine pitch demands. Furthermore realized applications will be presented, focusing on package realization and RF modules.
The technical and industrial issues associated with industrialization of embedding technologies will be announced briefly.

LAMINATED PACKAGE EMBEDDING TECHNOLOGY

Embedded chip package

The basic structure of a package realized by chip embedding is illustrated in Figure 1. The embedding technology focuses on the use of standard printed circuit board processes. The main advantage of such processes is the capability of using large substrate sizes for the package manufacturing and by that a significant cost reduction. By using thin silicon dies and a direct interconnect with micro via very small and thin packages can be realized, enabling a further miniaturization of the final application.

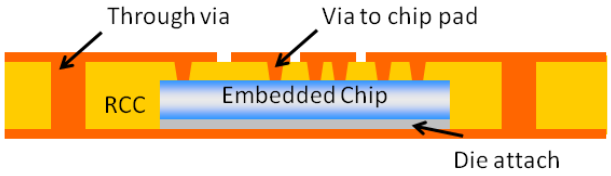


Figure 1. Embedded chip package, principle

Technology description

Wafer preparation

Laser drilling of microvias and the PCB metallization process is not compatible with Al or Cu contact pads of semiconductor chips. Therefore, a further layer of 5 µm Cu is applied to the bond pads of the chips to be embedded. Other metallization such as electroless Ni/Pd were optimized for microvia drilling and plating, and show the potential to avoid the additional galvanic copper metallization in the chip pads.

Passivation layers can be tested for their fragility as well as for their adhesion with the RCC laminate layers.

Die placement

In the beginning a core substrate needs to be prepared. This can either be an organic or non organic material. Figure 2 illustrates the process sequence.

On the substrate, thin chips are die bonded (a). Chip bonding has been developed by using printable pastes and die attach films (DAF). Screen printing allows a precise control of volume and location of the adhesive paste, which is rather a problem for dispensing. Electrically conductive Ag-filled pastes or B-stage pastes can be used. Another method is the use of a die dicing attach film (DDAF). It is a UV dicing tape which has two layers, a conventional UV dicing foil and an adhesive layer on top. Wafers are mounted on the adhesive layer. The dicing blade has to cut the silicon and the top layer of the tape. In the picking process this layer remains at the chip and serves as adhesive. Die attach films have shown superior adhesive coplanarity than pastes which is extremely important for precise epoxy thickness over the chip after RCC lamination and planar chip placement for avoidance of chip cracking. The challenge is to achieve the required die bond accuracy on a large substrate format. By using a Datacon evo placement and bonder machine a placement accuracy of ±10µm at 3σ was achieved on 18”x12” panels.

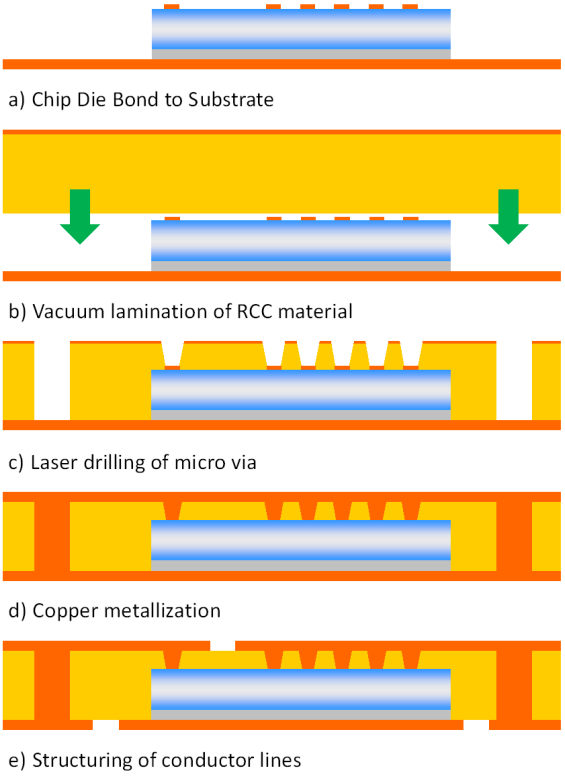


Figure 2. Process sequence for embedded package

RCC Lamination

Following the die bond process a dielectric film material (Resin Coated Copper / RCC) is vacuum laminated on the core substrate (b). It is preferred to keep the buildup construction symmetric to avoid a strong warpage of the whole substrate. The vacuum in the lamination chamber ensures a void free distribution of the dielectric material. The used vacuum lamination press is standard PCB production equipment. The lamination parameters like pressure and heating ramps need to be controlled carefully to avoid any damage to the chip. Detailed description of the lamination process is given in [8]. The whole lamination stack needs to be buffered using suitably soft materials. New developments in RCC laminates can improve significantly the adhesion on the chip surface and the reliability of the embedded packages by new epoxy formulations with adjusted thermo mechanical properties.

Micro via formation

Subsequently to the RCC lamination on the substrates, micro via contacts to the chip pads and to the substrate, and through holes to the backside are made. This is done by laser drilling (c). In a prototyping and R&D environment an UV laser machine is used. This type of laser is able to ablate the copper layer as well as the epoxy resin, enabling a very flexible processing of different materials. For a volume production environment the use of a combined UV/ CO_2 laser machine will enable the highest possible throughput.

With such a dual beam machine first the top Cu layer is opened by a 355 nm UV laser, cutting only slightly into the dielectric. Then a fast ablating CO_2 beam drills down to the bump, without attacking the Cu. The fast CO_2 laser allows drilling with speed up to 1500 holes/s. Another possibility would be to mask the copper with a photo resist mask and etch the copper at the micro via locations, following by the fast CO_2 laser drilling step.
In order to realize the electrical contact to the chip bond pad and to the substrate, copper metallization of the via contacts is done (d). To guarantee a defect free connection between chip bond pad and the via metallization a suitable cleaning step (desmear) is required, which removes remaining organic material from the pad, while roughing the dielectric surface to ensure a good adhesion of the metallization. A direct plating process is used in order to activate the polymer surface in the micro via for the electrolytic copper deposition. During this process a conductive palladium colloid is deposited on the epoxy surface only, which allows a direct metallization with an electrolytic copper bath.

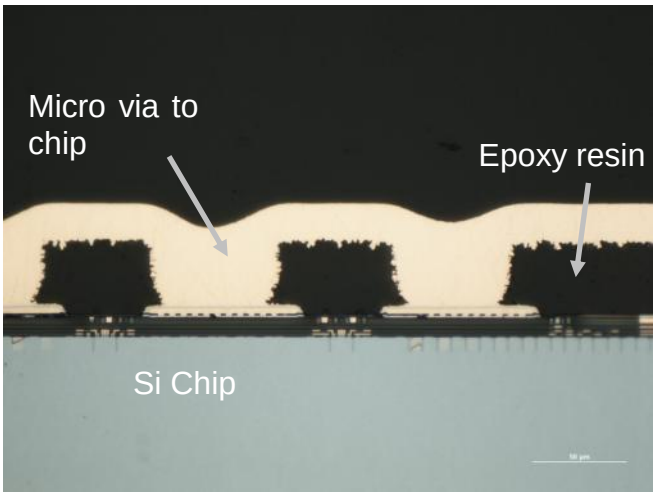
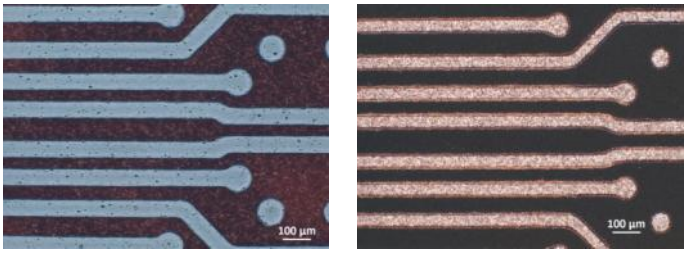


Figure 3. Metalized micro vias with 120 µm pitch.

Copper structuring
The circuit patterning (e) can be realized in different ways. One possibility is to use a laser direct imaging (LDI) of photo resist followed by an acidic spray etching.
Therefore a dryfilm photo resist is laminated and exposed by UV.



a) **b)**

Figure 4. Copper patterning a) resist mask b) copper etched

In Figure 4 an example for a 50µm lines and space pattern is shown.

This method realizes the fine pitch requirements of the embedded dies technologies, due to the possibility of local alignment of the structured pattern.
The final step of package realization is the separation using a laser or the standard (wafer) saw.
Figure 5 schematically summarizes the overall process flow. If this technology will be added to a PCB supplier, the process chain will require changes. The supplier will need to do assembly (requiring the respective machinery and training of the operators), and also needs increased depth in testing of the boards. Another possibility would be the addition of a complete process chain into an existing packaging facility.

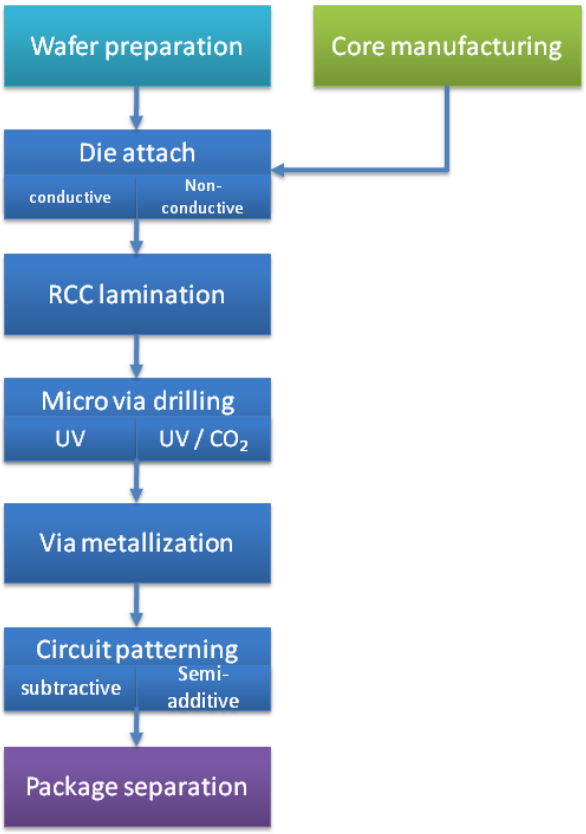


Figure 5. Process flow for chip embedding.

ULTRA FINE PITCH DEVELOPMENT

Challenges

In the HIDING DIES project, the feasibly of embedding dies with a peripheral pad pitch down to 100 µm pitch has been demonstrated for prototype. Currently most of applications requiring pitches in this range are possible to process with laser micro via without an additional redistribution layer on top of the die. However the target for the HERMES project is to realize demonstrators with a peripheral bond pad pitch down to 60 µm for prototype. These goals require the consideration of new approaches for connection the chip but also for the necessary re-routing. In the following different methods and already tested approaches will be described.

Embedded chip interconnect

The limiting factor for the laser micro via formation is basically set by the available laser drilling equipment. Current PCB laser drilling machine can realize drill diameters down to 30 µm diameter, as a result of the width of the focused laser beam. However, going down to bond pad pitches below 100 µm, beside die bond accuracy, also the precision of the laser positioning becomes an important factor within the series of all given tolerances. Therefore a connection that avoids a micro via becomes interesting.

A first method to realize an ultra fine pitch die embedding would be the use of an embedded flip chip (Figure 6). Here, instead of the laser micro via connections, the interconnects will be realized by an either soldered or conductively glued flip chip on the base substrate. The disadvantage of this method is, that no direct access to the back side of the chip is possible, which limits the possibilities for heat dissipation or electrical connection to the back side.

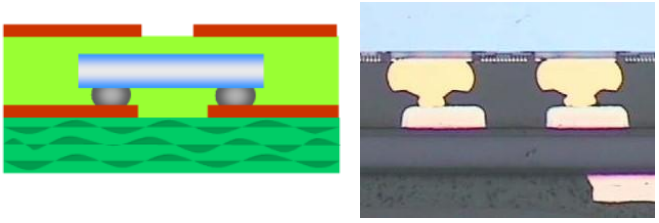


Figure 6. Embedded flip chip

A second method uses a silicon chip which is solder bumped prior to embedding. Here the die is bonded face up on the substrate, using a die attach method described in the process overview. During the vacuum lamination of the RCC foil, the solder bump is pressed through the epoxy resin and will form an electrical connection to the copper layer of the RCC material (Figure 7).

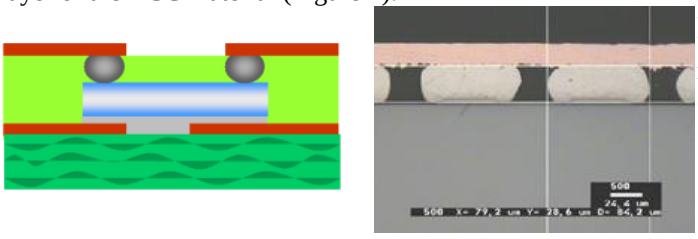


Figure 7. Vialess solder bump

Another approach that uses a face up bonded die is shown in Figure 8. Here a chip with gold stud bumps is die bonded prior to the RCC lamination. During the vacuum lamination process the Au stud penetrates through the epoxy resin into the copper layer, forming the electrical contact. For both methods a very well thickness control of the RCC above the chip is essential, in order to realize reliable interconnects. Feasibility tests have already shown the potential of these connection variations.

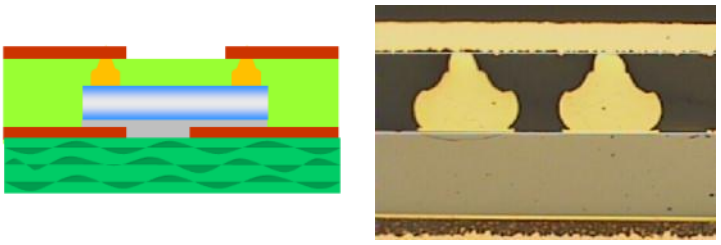


Figure 8. Vialess Au stud bump

Copper ultra fine line patterning

For the realization of fine line structures the described laser direct structuring method reaches its limits. Complexity of the needed patterns and large panel formats also reduce the throughput dramatically as a result of very long process times.

A Laser Direct Imaging (LDI) system enables finer structures, by the use of a dry film photo resist and the exposure by direct writing with the UV laser beam.
Currently available systems provide a resolution down to 15 µm lines and space on large substrate sizes with the possibility of local alignment. Figure 9 illustrates the basic principle of a LDI exposure of photosensitive films. The exposure is done by scanning of the highly focused laser beam on the substrate surface. Large panel sizes up to 24 by 32 inches can be processed with such equipment.
The LDI system provides two major advantages: registration accuracy and flexibility.
The registration accuracy is capable to use dynamic registration that enables necessary image adjustment, considering possible substrate warpage and deformation, prior to resist exposure.
No need of exposure masks provides the highest level of flexibility. New Layouts and design modifications can be realized easily by simple changing the software, avoiding costly manufacturing of masks.

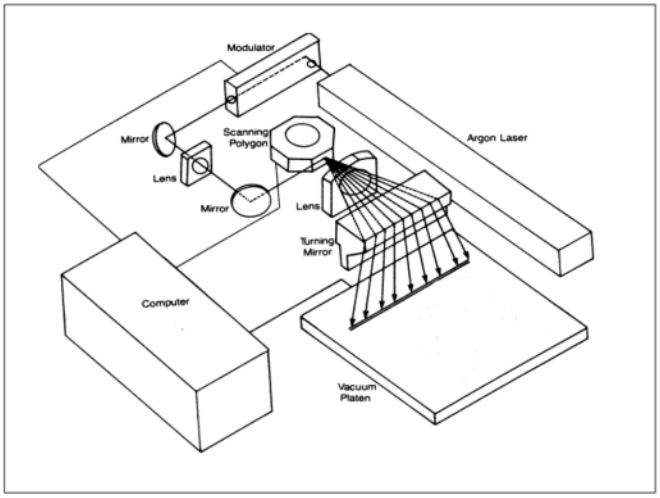


Figure 9. LDI principle (Source: Orbotech)

The availability of high intensity laser beams in combination with very sensitive photo resist materials

enable a very fast processing. Dry film resist materials that are optimized for LDI exposure are available by different suppliers. These materials require exposure energies in the range 12 to 20 mJ/cm², and are available in film thicknesses down to 15 µm. This will allow the realization of structures down to 15 µm lines and space. Going down to these fine feature sizes, treatment of the substrate surface, which is usually copper, becomes a very important process step, to ensure a good and reliable resist adhesion after exposure and development.

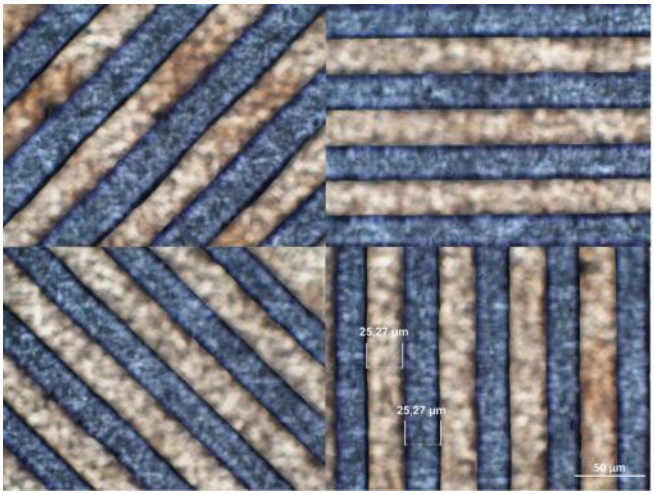


Figure 10. Test pattern exposed by LDI

In Figure 10 a test pattern realized with LDI exposure are shown. The used dry film was not optimized for LDI. Nevertheless it was possible to achieve a resolution down to 25 µm lines and space in a 15 µm thick resist. Pattern reproduction was observed regularly and adhesion of these structures was excellent.
Under etching issues restrict the capability of structuring even finer structures by a subtractive process. Very fine L/S of 15-25µm have the need for semi-additive processes. In this challenge, the plating and base copper etching need to be controlled well to facilitate the creation of very fine Line/space structuring. The copper foil will be laminated with the epoxy resin as an RCC again, following by the production of a LDI exposed photo resist mask. Copper will be electroplated in the patterning and finally the thinner base copper can be etched more easily after resist removal.

APPLICATIONS

Embedded power MOSFET package

In cooperation with NXP an embedded power MOSFET package has been realized as one technology demonstrator of the HIDING DIES project. The goal was to use the embedding technology based on dielectric lamination to realize a thin, cost effective SMD package.
The vertical power MOSFET device has contacts on both sides which make a further thinning of the semiconductor not possible.
For electrical contacting the back side contact of the transistor, the dies are die bonded with solder on a 36 µm copper foil (Figure 11). By that an excellent thermal contact to the chip is realized also, which enables a good heat flow out of the package.
The die thickness of the power transistor chip was 150µm. A prepreg with holes corresponding to the dies is aligned onto the foil assembly to compensate the die thickness. On top of the prepreg and the dies a resin coated copper foil is applied. The stack is then laminated and cured under vacuum.

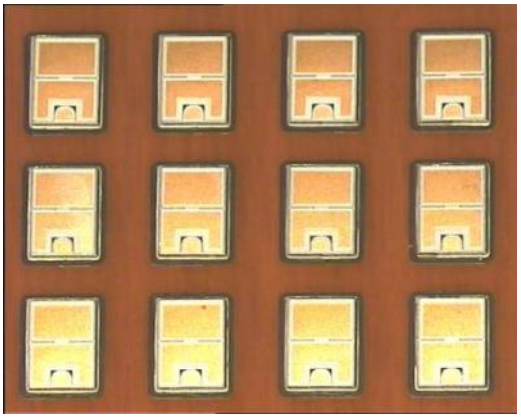


Figure 11. Die bonded chips on Cu substrate

Micro via contacts to the chip pads and the copper substrate are made by UV laser drilling and electrolytic copper deposition. The final copper patterning is realized using a laser direct structuring step, followed by alkaline etching of the copper.

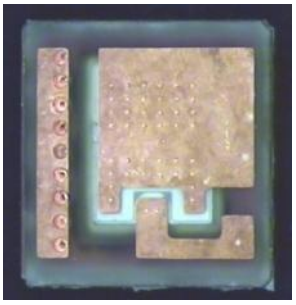


Figure 12. Embedded power MOSFET.

After separation the final package has a size of 3,3 by 3,3 mm². An example is shown in Figure 12.
The total thickness of the package, which can now be assembled like an SMD component is about 200µm.

Radar module

In the German project KRAFAS, which is coordinated by Bosch, the goal is to realize an embedded adaptive cruise control module, with the focus on cost reduction in combination with the same or better performance than the existing system.

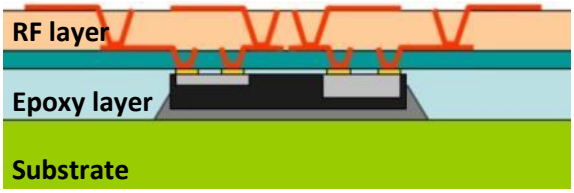


Figure 13. Schematic of embedded radar module

Figure 13 shows the schematic of such a embedded radar module. Beside the epoxy material, in which the molded dies are embedded and a fan out is realized, an additional layer of RF material is required to maintain the RF performance of the system. The challenge here is the combination of these both materials and processing them in the same PCB process flow. In Figure 14 a demonstrator example for such a module with the realized final RF layer is shown.

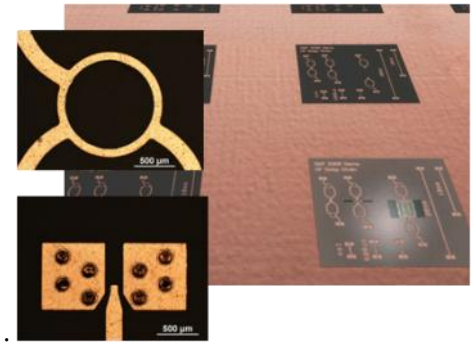


Figure 14 Structured RF layer of 77 GHz test module.

Successful processing of the RF material in combination with the existing "Chip in Polymer" process flow was demonstrated. First realized embedded devices have been tested and showed an excellent performance at 77GHz, superior to the existing interconnection technologies. A cost reduction potential of about 30% is estimated by using this technology.

New package developments

New developments aim to realize further new packages, which use the electrical and cost advantages of the embedded die technology.
Currently different developments are in progress.

Single die packages

The first is a Quad Flat Nonlead (QFN) like embedded package. The goal is to realize an ultra thin QFN package containing an embedded die, which is produced using chip embedding technology on a large panel format. The goal is to realize packages that can be compared with standard QFN packages in terms of performance, reliability and handling, providing the same form factor with reduced thickness and a lower manufacturing cost.

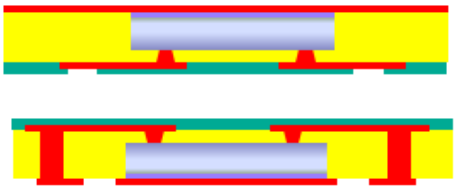


Figure 15. QFN variation A and B

In Figure 15 a drawing of two different variations of such a QFN package is shown. In the first step, the used die has a peripheral bond pad pitch of 100 µm. The variation A realizes a redistribution of the chip bond pads to the peripheral QFN pads at 400 µm pitch and contacts the chip by laser microvia.
Variation B also incorporates routing of the contacts to the backside of the substrate using through contacts, realizing a standard QFN footprint including the thermal die contact in the middle. Both variations can realize lowest possible thickness of the final package.
In addition a BGA type package will be realized (Figure 16)

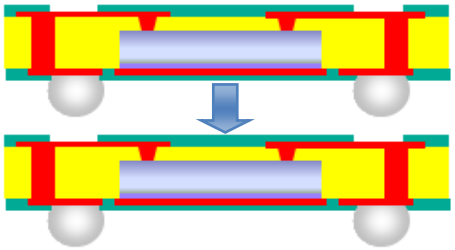


Figure 16. Stackable BGA package

The basic construction is similar to the QFN package B, but a stacking and testing of multiple packages will be possible with this variation.

Multi die package

Another is the realization of multi die packages. In the first approach dual chip modules will be realized.
The challenge here is advance the existing technology to multiple die bond and lamination steps.
Figure 17 schematically illustrates a dual chip package. Subsequent die bonding and lamination cycles were performed with the required die bond accuracy and without any damaging of the thin silicon dies during multiple lamination cycles. The use LDI for resist exposure and semi additive circuit patterning helps to achieve the higher demands in complexity for such a package.
Within the framework of new industrial and EU funded projects, currently first prototypes are under realization. The focus here is also on an industrialization of the whole process chain.

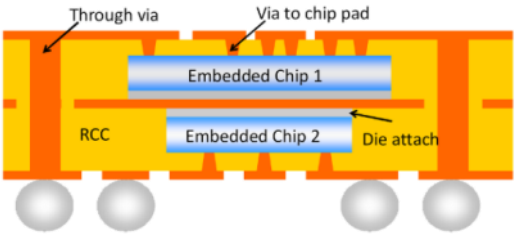


Figure 17. Embedded dual chip package

CONCLUSIONS

The Chip in Polymer technology results in the embedding of active silicon die into the build up layer of standard PCB substrates. The main process technology steps are adapted from standard PCB processing to implement a cost effective approach for an embedding technology.

Currently projects focus on the application of the Chip in Polymer technologies for the manufacturing of small packages like stackable chip packages, SiPs or small modules with only a few chips. The maximum number of embedded chips will be determined by the yield, which means cost at the end.

In the result for the chip embedding technology, the semiconductor chips are fully embedded into a flat package, which can be handled like a standard SMD component then.

The changes in the process chain are an immense challenge for a traditional PCB manufacturer. To face this challenge and to move forward towards industrialization, the new European project HERMES will focus mainly on industrial adaptation of embedding technologies.

Industrialization of embedding technologies is the next step taken after the successful validation of embedding technologies at prototype level. New efforts try to set up a new business model by merging the segments of PCB manufacturing and component assembly. The goal is a new integrated manufacturing line to offer low cost solutions for high density electronic systems.

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REFERENCES

[1] R. A. Fillion, W. E. Burdick, Ch. E. Bauer, Ph.D., Herbert J. Neuhaus, Ph.D., “High Performance, High Power, High I/O Chip-on-Flex Packaging”, EMPC 2005, June 12-15, Brugge, Belgium

[2] H. Braunisch, S. Towle, R. Emery, C. Hu and G. Vandentop, “Electrical Performance of Bumpless Build-Up Layer Packaging”, Proc. ECTC 2002, May 28. - 31. 2002, San Diego, USA.

[3] P. Palm, R. Tuominen, A. Kivikero, “Integrated Module Board (IMB); an Advanced Manufacturing Technology For Embedding Active Components Inside Organic Substrats, Proc. ECTC 2004

[4] V. Chiriac, B. Keser, L. Larsen, L. Ramanathan, D. Trung, "Thermal Performance Evaluation and Optimization for Redistributed Chip Package (RCP) Designs", 4th International Conference on Device Packaging, Scottsdale, March 17-20, 2008.

[5] L. Boettcher et. al., “Integration of active and passive components using Chip in Polymer technology”, SMTA International, Chicago Il., Sept. 25. – Sept. 29. 2005

[6] HIDING DIES website: http://www.hidingdies.net/

[7] Session T-A-1C. “European Projects on Embedding of Actives and Passives” in Proceedings of the 16th European Microelectronics and Packaging Conference, Oulu, 2007

[8] D.Manessis, S-F.Yen, A. Ostmann, R. Aschenbrenner and H. Reichl, “Technical Understanding of resin-Coated-Copper (RCC) lamination processes for realisation of reliable chip embedding technologies”, Proc. in Electronics Components & Technology Conference (ECTC) 2007, Reno, NV, May 29-June 1, 2007, pp. 278-285.